IMA: technical foundations, application and performance analysis

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Abstract

Using WAN established infrastructure, one of the main problems ATM network planners and users face, when greater than T1/E1 bandwidth is required, is the disproportionate cost associated with T3/E3 links. The technology to cover the gap between T1/E1 and T3/E3 bandwidth at a reasonable cost is known as inverse multiplexing for ATM (IMA). IMA allows multiple T1/E1 lines to be aggregated to support the transparent transmission of ATM cells over one single virtual trunk. In this paper, the fundamentals and major applications of IMA technology are described. Also, the behavior of IMA multiplexers is carefully analyzed and a method to dimension them proposed. For this purpose, an IMA simulation tool has been developed. The IMA simulator permits the study of individual devices and the evaluation of the end-to-end performance of a logical trunk under several ATM input traffic patterns. The analytical study is based on the comparison with an $M/D/C/(N + C)$ queue system. Under Poisson input traffic, an approximation for the cell loss ratio (CLR) is derived and an estimate of the cell delay in an IMA multiplexer obtained. In addition, the suitability of these results for two types of bursty traffic is investigated. © 2001 Elsevier Science B.V. All rights reserved.

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1. Introduction

The growing demand for high speed services is accelerating broadband integrated services digital network (B-ISDN) deployment to support conventional and new data, voice, video and multimedia applications in a single network. This network is based on the asynchronous transfer mode (ATM) to carry any type of traffic efficiently.

The dominant role of ATM in the LAN scenario is still unclear in comparison with other competing technologies such as switched Ethernet, Fast Ethernet and even Gigabit Ethernet. ATM is well introduced in the backbone area, especially in private corporate environments. Regarding WAN,
network operators are first providing access to the ATM network using the existing infrastructure and then gradually deploying the new one, implementing pure ATM interfaces over it. Users, however, want the ATM bandwidth benefits for their high speed applications soon, but in a cost-effective manner.

Currently, there are basically two available options to provide access to the ATM services on a WAN scale. One consists of T3/E3 links offering considerable bandwidth (44.736/34.368 Mbps) but is usually not justified since it would be underutilized by most of the prospective users. Furthermore, the rates that carriers charge for them are very high. The other alternative is substantially cheaper and uses T1/E1 links (1.544/2.048 Mbps), but the offered bandwidth is insufficient for some user needs.

Prices depend on several factors such as distance and each particular carrier. As an example, the average cost per month of a 25 km T1/E1 link is $850/$2900, respectively, and $7500/$29,000 for a T3/E3 line of the same length [7]. However, in general, T3/E3 links have their point of presence and are only available in big cities [7,14]. Due to cost and availability of service, an intermediate solution offering enough bandwidth at a reasonable cost is required.

In July 1997, the ATM Forum published the inverse multiplexing for ATM specification, known as IMA [3], the last version of which was released in April 1999 [4]. IMA defines the transparent transmission of a high speed ATM cell stream over one logical link composed of several T1/E1 lines. IMA distributes and transfers a single flow of ATM layer cell traffic onto multiple physical links. At the remote end, the traffic is recombined and the original ATM cell sequence fully recovered and delivered to the higher layers that will further process it. Up to 32 T1 or E1 links can be used to form an IMA group that operates at an aggregated bit rate of some multiple of the T1/E1 speed. Up to 48/64 Mbps can be reached. These bit rates are enough to support many current user broadband applications requiring a fractional T3/E3 bit rate but using bandwidth more efficiently, and utilizing readily available and less expensive T1/E1 services.

The inverse multiplexer (IMUX) is the device responsible for grouping several T1/E1 physical circuits into a single logical trunk. An IMUX accepts ATM cell streams coming from different traffic sources, in addition to traffic coming directly from LANs (e.g., from a router without an ATM interface). This non-ATM traffic is adapted and converted to ATM cell format, using ATM layer segmentation and re-assembly functionality. In both cases, the IMUX distributes the resulting cells in round-robin fashion over the physical links maintaining the QoS required by each individual connection. To configure, control, maintain and synchronize the links belonging to an IMA group, the IMUX introduces two types of operation and maintenance (OAM) cells. That is, IMA control protocol (ICP) and Filler cells.

Thus, in this paper, the origins, application and technical foundations of inverse multiplexing are explained in tutorial style. Then, a model for an IMUX is presented and intensively evaluated. To perform the evaluation under different input traffic distributions an IMA system simulator was developed. The idea was to elaborate a methodology to help engineers and network planners to characterize and dimension an IMUX device, that is, to obtain the buffer size and the number of T1/E1 output links that guarantee the required QoS parameters demanded by users, basically measured as cell loss ratio (CLR) and average cell delay. An approximate analysis allowing easy computation of the IMUX performance was derived, obviating the need to perform costly simulations. The IMUX dimensioning study was conducted under Poisson input traffic. More realistic traffic patterns are also presented in this study. Due to their simplicity, we decided to use two models of bursty traffic instead of those described in other surveys [5,9,19,20]. These bursty models are an on–off pattern [6], and a WWW traffic characterization [11] for residential networks. Of course, the usefulness of these patterns is limited to certain scenarios (e.g., Poisson traffic is a characterization of multiple traffic aggregations), but equally obviously, the performance of the IMUX is traffic dependent. For this reason and since the actual traffic behavior is subject to short-term future changes depending on user requirements, we present this study as a more
“permanent” way to model IMUX performance. This research attempts to help engineers to validate and verify their device node libraries (IMUX in this case) in the network simulators they have to develop, since no other means (e.g., mathematical analysis) is now available in a closed, useful and easy manner to plan broadband networks in a traffic changing environment. Although several relevant traffic characterization advances have been achieved, they show well-known characteristics (e.g., its self-similar nature), and the resulting models are too complicated to help in the analysis of emerging devices and networks. Once these libraries are validated, engineers can evaluate IMUX performance with more realistic, but changing, traffic patterns.

The paper is organized as follows. Section 2 discusses the current knowledge regarding IMUX operation and its main applications. The simulation model is introduced in Section 3. The study under Poisson input traffic is presented in Section 4. This section also includes the approximate analysis for the CLR and the average cell delay. The results for bursty traffic are described in Section 5. Finally, Section 6 summarizes the main conclusions of this study and outlines some future work.

2. Inverse multiplexing fundamentals and network applications

In a conventional multiplexer, various independent input channels are combined into one high speed link for efficient transmission. The situation changes when existing applications and local traffic have the opposite requirement. Users have high speed LAN data, video-on-demand, multimedia applications, etc., to interconnect, interact and interoperate between remote ends. They can lease a wide-bandwidth circuit (e.g., T1/E1 or T3/E3) but its capacity has to be fully used over time to justify its cost. As an alternative, a cost-cutting scheme can be used. The original idea was based on leasing a number of small bandwidth synchronized digital telephone circuits (56/64 Kbps) to obtain a higher speed connection, the capacity of which is approximately the sum of link capacities minus a small amount of overhead. Therefore, the transmission of a wider-bandwidth signal is possible over the existing switched digital telephone network on a dial-up basis. This process is the reverse of multiplexing, because it involves breaking a wider signal into multiple smaller capacity and independent channels for transmission. Furthermore, the customer uses the minimum required bandwidth (with the granularity of the channel rate) and for the minimum necessary time. In addition, he has the flexibility to use as much or as little bandwidth as needed on a demand basis. Finally, the user has only to pay for the time bandwidth that is consumed. Inverse multiplexing for ATM follows this scheme, but using multiple T1/E1 links to constitute an IMA group of the required high speed to bear ATM services.

As Fig. 1 shows, there are other alternatives to employ several T1/E1 links for WAN connections, e.g., load sharing. Inverse multiplexing and load sharing are similar in the sense that they use various T1/E1 lines. However, while inverse multiplexing combines these lines into a single logical connection, load sharing handles them as separate links. Load sharing can be implemented according to two options, route caching and frame-by-frame. Route caching assigns each individual connection to a particular T1/E1 link; therefore, any given application has its bandwidth limited to the data rate offered by that link. In addition, by using such a strategy an entire connection is lost if a physical failure occurs.

In the frame-by-frame option, each packet is individually routed over one available T1/E1 line. Accordingly, there is no bandwidth-per-application limitation, except for the total number of T1/E1 links leased. However, the receiving router

![Fig. 1. Inverse multiplexing vs load sharing.](image-url)
has to reorder packets that can be received out of order due to different delays occurring among the links. This increases the hardware complexity of the receiver as well as the processing time and, therefore, the system latency (i.e., the receiver has to read the buffers and reorder the cells, testing the queues until the next cell is found). In IMA, cells are delivered to the links in round-robin fashion, which implies a simple receiver implementation that only has to read cyclically the delay compensation buffers (DCB in Fig. 7) used to balance the different delays among the links. Inverse multiplexing also has additional advantages over load sharing. For example, if link failures happen, then the connections involved can still be preserved, although at the price of temporarily reducing the total bandwidth assigned. The failing T1/E1 links are automatically recovered and returned to the IMA group when they are restored. Consequently, inverse multiplexing continues to offer service to the applications although the QoS is deteriorated for the duration of the failure. Furthermore, inverse multiplexing could offer bandwidth on demand, dynamically adding more T1/E1 links to a session in progress if more bandwidth is requested. Circuits could be removed when the bandwidth is no longer needed. Currently, this is one of the ATM Forum sub-working group goals.

The three typical network configurations to which IMUX technology applies are depicted in Fig. 2. The three types are: access connection to the ATM network, internal network-connection between ATM switches, and dedicated bandwidth connection between two remote ends (ATM leased line IMA).

One type of real IMA application [2], in which the required rates are between T1/E1 and T3/E3, is integrated access over ATM (Fig. 3). In this scenario, a remote customer requires a way to integrate multiple services at a single location to reduce the access and maintenance costs. Another possible application is service and switching concentration. Service providers that are moving to supply new services find that the initial requirements are not enough to justify large-scale multi-service switching concentrators. With IMA, they can scale their networks as their subscriber base grows.

IMA could be used to link together ATM islands in a cost-effective manner, allowing the addition of ATM WAN bandwidth in T1/E1 increments (Fig. 4). In public video distribution services (Fig. 5), IMA offers a solution for the efficient use of bandwidth. Video services are only active for a fraction of time, and for this reason it is inefficient to reserve this bandwidth all the time. With the dynamic bandwidth allocation feature, IMA could use only the needed bandwidth and the

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**Fig. 2.** Typical network configuration using IMUX technology.

**Fig. 3.** IMA transmit end.

**Fig. 4.** IMA solution for linking ATM islands.
rest could be used by e-mail services and Internet access. Dynamic bandwidth is one of the future goals of the IMA specification working group.

IMA is a process in which an ATM cell stream is cyclically distributed onto multiple T1/E1 physical links as shown in Fig. 6. The original flow is re-assembled at the receiving end. To control the different physical links and to reconstruct the ATM cell stream the ICP protocol is employed. The IMA control protocol uses special OAM cells or ICP cells that are periodically inserted in each line. These cells carry information regarding the state of the link, the number of links being multiplexed, when to add or remove a T1/E1 link from an IMA group and the differential delay values among links. Also, ICP cells provide the definition for an IMA frame. An IMA frame on each link within the IMA group consists of $M$ consecutive cells (from 0 to $M - 1$), one of them being an ICP cell. The value of $M$ is configurable and its default value is 128. In this case, an ICP cell is normally introduced every 127 cells $[3,4]$. As the ICP cell insertion is periodical, the position of an ICP cell in the IMA frame is fixed. It allows the receiver to arrange IMA frames that arrive unaligned due to different delays occurring in each individual link.

The IMA protocol also defines a new OAM cell, the Filler cell. Filler cells are appropriately injected to provide cell rate decoupling between the bit rate of incoming ATM layer cells and the IMUX operation nominal rate. This rate is known as the IMA data cell rate (IDCR) and it is defined in $[3,4]$ as follows:

$$\text{IDCR} = C \times \text{TRLCR} \times \frac{M - 1}{M} \times \frac{2048}{2049},$$

where $C$ represents the number of links in the IMA group, and TRLCR is the timing reference link cell rate. The TRLCR is the rate of one of the output links (E1 link rate) which is used to pass synchronization from the transmitting to the receiving end. It is derived from one of the physical links identified as the timing reference link (TRL), which is used for synchronization purposes. The $(M - 1)/M$ factor accounts for the scheduling of an ICP cell every $M$ cells. Finally, the ratio $2048/2049$ refers to the insertion of one “stuff event” (two consecutive SICP cells) every 2049 cells. It is required to prevent de-synchronization among links operating with independent clocks. Stuff ICP (SICP) cells provide some tolerance to compensate clock divergences. This is accomplished by introducing two consecutive ICP cells (SICP cells) every 2048 ICP, Filler and ATM layer cells in the TRL

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Fig. 5. IMA solution for public video distribution services.

Fig. 6. IMA transmit end.
reference link, and SICP cells in the remaining links as needed.

Fig. 7 represents the IMA receiver. It is responsible for aligning IMA frames and buffering them to recombine the traffic back into the original ATM layer cell sequence. Reception buffers are cyclically read at the IDCR rate. The reading process is controlled by the IMA cell clock at the IDCR rate. DCBs are read in a round-robin order. When an ICP cell is found, the round-robin receiver ignores it and immediately advances to check the next link until a FILLER or ATM Layer cell is found. Analogously, when a stuff event is found, the two SICP cells are ignored. These control cells are suitably processed by the IMA control protocol. If the round-robin receiver finds a Filler cell, it is discarded and the IMA waits until the next tick of the clock. If it is an ATM layer cell, then it is passed to the ATM layer.

3. IMA characterization and simulation model

The system modeled for this study is illustrated in Fig. 8. To examine IMA operation under different traffic patterns, load conditions, number of output links and different buffer sizes an IMA simulator written in C++ object-oriented programming language has been developed [17]. It simulates independent IMUX devices (sender and receiver) as well as a complete end-to-end IMA group.

The system is composed of a traffic source, an ATM inverse multiplexer, a variable number of transmission links, an inverse de-multiplexer and a traffic collector.

Three traffic patterns are available in the current version: Poisson cell arrivals and two bursty traffic models, on-off traffic and a WWW traffic characterization for residential LANs [11]. Input traffic of variable load attacks the IMUX device that operates at the IDCR rate. The IMUX can be configured to have C output ports each running at the TRLCR data rate. All output ports are perfectly synchronized. The number of IMA links is variable, although typical commercial values range from 2 to 8, because for higher values, it is cheaper to lease a T3/E3 line. The IMUX device implements buffering of selectable size to temporarily store ATM layer cells in case they cannot be immediately injected into the output ports. Control cells (ICP, SICP and Filler cells) are considered not to occupy memory since they are generated at the same time they are transmitted. The queue size depends on the number of arriving ATM layer cells, and is limited to the total memory pool assigned to the IMA device. The memory is thus

![Fig. 7. IMA receive end.](image)

![Fig. 8. IMA system model.](image)

![Fig. 9. Mercury organization at the IMA multiplexer.](image)
shared among all output ports. A cell is only lost when the memory is completely full of ATM layer cells. As Fig. 9 shows, the ATM layer cells are distributed onto the output links, at the IDCR rate, according to a round-robin algorithm. Also, the accurate introduction of control cells for their respective output ports is indicated. The memory at output ports is employed to schedule the departure of cells, and it is a part of the total memory of the IMUX. This memory is used on demand. For this reason, empty buffers available for the incoming cells are only present at the input queue of the system. No real output queues are dedicated to every output port. Therefore, the FIFO queues at output ports depicted in Fig. 9 are only a logical representation. In this study, the total shared memory is fixed and the IMUX behavior in terms of losses and delay is measured.

The IMUX output ports go through a network of links that only simulates a different length for the links in the IMA group. Therefore, the impact of different delays on the cell delay and cell delay variation can be examined. However, in this study all the lengths are considered identical. Consequently, the end-to-end delay will be the minimum, since for different lengths, the receiver would have to wait for cells arriving at the buffer of the longest link.

At the remote end, the IMA de-multiplexer receives the C lines and reconstructs the original cell stream. Incoming cells are stored in DCBs, one for each link, and are then cyclically read at the IDCR rate.

The simulation tool includes three different traffic sources (Poisson, on–off and a WWW traffic characterization in residential networks) which are described in the following sections.

4. Performance evaluation under Poisson input traffic

To study the IMUX behavior and develop a methodology to assist in its dimensioning, some parameters have to be considered. The number of output links in the IMA group is decided as a function of the required bandwidth. The amount of buffering has to be estimated according to the main QoS parameters contracted. Here, the CLR and the average waiting time for the ATM layer cells in the IMUX are used. Also, the buffer size depends on the input traffic pattern and the load applied to the IMUX device. In this section, we compare the results obtained by simulation with those obtained from a proposed mathematical analysis that allows easy IMUX dimensioning without the need for costly simulations. To gain insight and simplify the analysis, we consider that ATM cells arrive at the IMUX according to a Poisson process. As a result, IMUX operation can be related to the discrete-time behavior of an $M/D/C/(N+C)$ queuing system. In this study, we first examine the main differences between an IMUX device and an $M/D/C/(N+C)$ system. The excess of cell losses observed in the IMUX regarding the CLR derived from the mathematical analysis is further modeled. Then, the $M/D/C/(N+C)$ system is tuned to approximate the simulated CLR. Finally, the same $M/D/C/(N+C)$ characterization is also used to estimate the mean waiting delay in an IMA multiplexer.

The number of generated cells in an interval of time $[0,t]$ is given by a Poisson process of average $\lambda t$, where $\lambda$ is the average ATM cell generation rate. Particularizing for an IMA system, a Poisson source generates cells at average rate $\lambda$, and the IMUX is loaded by a factor $\rho$ given by the expression

$$\rho = \frac{\text{Poisson rate}}{\text{IMA rate}} = \frac{\lambda}{\text{IDCR}}. \quad (2)$$

In general, (2) is also valid for any type of traffic, where $\lambda$ is the mean number of cells generated by unit of time. In ATM, the time is usually normalized to the transmission time of an ATM cell.

4.1. CLR estimate in an IMA multiplexer using an $M/D/C/(N+C)$ system

Assuming Poisson input traffic and the same amount of available resources, $C$ output links and an input queue of finite size $N$ cells, the actual IMA multiplexer and its $M/D/C/(N+C)$ representation are, a priori, similar. Both have $N$ memory positions to hold $N$ cells and they possess
C identical output ports (servers), each with a constant service time (ATM cells have fixed size). Time is slotted into fixed length slots and, to simplify the analysis, the slot is taken as unity. The treatment of priorities and scheduling policies to support different traffic classes is beyond the scope of this paper.

The two systems differ in how incoming cells are processed and sent to their respective output link. In an $M/D/C/(N+C)$ system only ATM layer cells are served, but in an IMUX, protocol cells (ICP, SICP and Filler) are also inserted and delivered. Although it may be considered that Filler cells are also transmitted when there are insufficient ATM layer cells in a $M/D/C/(N+C)$ model to serve, therefore fulfilling the cell rate decoupling function, there still remain some further differences, as is explained below. In addition, in an $M/D/C/(N+C)$ system, ATM layer and control cells are not cyclically distributed over the $C$ output links.

Let us analyze first the effect produced by ICP and SICP cells (two consecutive ICP cells in the same output link). As can be seen in Fig. 10, an ICP cell is inserted in all links every $M = 128$ cells with a given different offset for each link.

The IMA specification [3,4] recommends ICP cell insertion within each IMA frame on a physical link at specific locations. Each ICP cell appears in a different slot within a frame on different links within the IMA group, but the position is the same from frame to frame on any given link. In particular, it is recommended to have an ICP cell insertion at slot 0 on link 0, slot $M/2$ (link 1), $M/4$ (link 2), $3M/4$ (link 3), $M/8$ (link 4), $3M/8$ (link 5), $7M/8$ (link 7), etc., $M$ being the IMA frame length (i.e., 128 slots).

Consequently, when an ICP cell is delivered the transmit IMA serves in this time slot ATM layer cells only on the remaining $C-1$ links. In comparison, an $M/D/C/(N+C)$ system always serves $C$ cells if there are more than $C$ ATM layer cells in its buffer. Therefore, under these circumstances, the real IMUX has to store one additional cell, contributing to an increase in the CLR with regard to that derived from the analytical model.

On the other hand, Filler cells are necessary to adapt the input ATM layer cell rate to the IMUX operation rate (IDCR), that is, to fill those links that cannot be provided with ATM layer or ICP cells. Thanks to this, the round-robin cell distribution synchronism is kept over the links and the receiver is allowed to recuperate the original ATM cell stream. In an $M/D/C/(N+C)$ system, cell delivery is always done at the end of a time slot.

Operating at the IDCR rate it may be that no ATM layer cell is available to schedule over an output line at the first decision time and a Filler cell is inserted instead. However, as Fig. 12 shows, $C$ or more ATM layer cells may arrive just after

\[
\begin{align*}
\text{Fig. 10. ICP and SICP cell insertion in an IMA group of four links.} \\
\text{Fig. 11. Cell delivery timing over } C = 4 \text{ links. } M/D/C/(N+C) \text{ model vs IMUX.}
\end{align*}
\]
this instant. Therefore, some ATM layer cell may accumulate within the IMUX buffers, negatively affecting the CLR. This phenomenon does not occur in an $M/D/C/(N + C)$ model.

An additional effect has to be considered. Cells are cyclically delivered at the IDCR rate but ICP cells have to be periodically inserted into a given output port every $M = 128$ cells. Therefore, when an ICP cell is to be inserted, the corresponding ATM layer cell will be placed onto the next available link (see cell number 1 in Fig. 13). This event delays the delivery of ATM layer cells. Consequently, an ATM layer cell (cell number 4) arriving to the IMUX before others is transmitted later, as illustrated in Fig. 13.

This has a noticeable impact on the mean delay. In addition, the incident lasts until the completion, during a time slot, of the distribution of $C - 1$ cells at the IDCR rate. Again, while some cells would normally be served by an $M/D/C/(N + C)$ queue, they still remain in a real IMUX, producing an increase in the CLR, average cell delay and cell delay variation (CDV).

Once the main differences between the IMUX and the analytical model have been stated, simulation results corroborate that mean cell delay and CLR in the IMUX are greater than those derived from the exact solution of an $M/D/C/(N + C)$ queue system. However, following this reasoning, three different approaches to tackle the estimate for the CLR can be considered.

- Increasing the load offered to the $M/D/C/(N + C)$ system over that applied to the IMUX, but maintaining the same number of output links and buffer capacity. Under these assumptions, the rate of ATM layer cell arrivals grows and the CLR increases.
- Increasing the number of links ($C$) in the queuing model over those in the IMUX. The offered load per link, the buffer size and the time slot size are kept invariable. In this case, if the applied load per link is maintained, as $C$ increases the total number of incoming ATM layer cells to the system by unit of time also increases, thus degrading the CLR.
- Reducing the buffer size ($N$) in the $M/D/C/(N + C)$ model below that assigned to the IMA system. If the offered load per link along with the number of output links do not change the CLR grows.

All the three options have been studied [1], but here we have chosen to present the last one. It is a reasonable choice, because to obtain an exact solution of the resulting $M/D/C/(N + C)$ queue model it is necessary to solve a system of $N + 1$ equations with $N + 1$ unknowns [8]. Therefore, a shorter queue reduces the number of equations and calculations simplifying the analysis.

To judge the magnitude of buffer reduction needed, several preliminary simulations were performed, varying the buffer size. The offered load per link ranges from 50% to 90% and $C$ takes values from 2 to 8, that is, traffic loads under normal operation and common output port values of commercial IMA systems. Examining the CLR values obtained, the required reduction in cells for the buffer capacity in the $M/D/C/(N + C)$ system to obtain an accurate approximation of CLR as a
function of the number of output links ($N_{\text{red}}(C)$) is shown in Table 1.

These results can be further approximated by a straight-line equation (3), where $\left\lfloor \cdot \right\rfloor$ represents the round function

$$N_{\text{red}}(C) = \left\lfloor \frac{5 \cdot C + 11}{7} \right\rfloor. \tag{3}$$

Figs. 14 and 15 plot the CLR under offered loads per link of 60% and 80%, respectively. Simulation results are represented by a dot corresponding to a given buffer size. The analytical values derived from the solution of the $M/D/C/(N+C-N_{\text{red}}(C))$ system are denoted by solid or dotted lines. Simulations were conducted in segments of two million cells. Due to the number of cells simulated, the 95% confidence intervals are only significant and visible for CLR values around $10^{-6}$. To consider CLR $\leq 10^{-6}$ with reasonable statistical confidence, it is necessary to simulate more than $10^7$ statistically independent cells, which would begin to be computationally very expensive. Therefore, to reach simulated CLR values of very small order (CLR $\leq 10^{-12}$), it would be necessary to introduce rare-event simulation techniques to accelerate the running time (e.g., the repetitive simulation trials after reaching thresholds (RESTART) simulation method [21]). Although it is beyond the scope of this study, our proposed analysis may be used to obtain a reasonable estimate for arbitrarily low CLR values.

As expected, the CLR depends on the applied load, number of links and buffer size. It is observed that the proposed approximation improves as the offered load and the buffer size increase. The approximate CLR values are always pessimistic in the sense that they are greater than the equivalent simulations. Nevertheless, this does not represent any obstacle for the IMUX dimensioning.

For a given buffer size, when the applied load grows the CLR increases since the number of cell arrivals is higher. As buffer size increases the CLR decreases, but more slowly as the offered load becomes larger. Also, as the offered traffic load grows the difference between leasing a smaller number of output links and a larger one becomes less effective because at high load the losses are also excessively high.

In addition, the CLR grows when the number of links ($C$) increases. This is because the simulated IMA multiplexer has all its output ports fully synchronized, thus performing service at the same time. In this way, a Filler cell must be delivered to the appropriate output link when no ATM layer cell is available at the beginning of a time slot.
Therefore, the emission of an ATM layer cell over that link, if any, will occur in the next time slot. Furthermore, assuming that the offered load per output link remains fixed, the input cell rate to the IMUX increases when the number of links grows. Hence, in a given time slot and for a fixed buffer size it becomes more likely to be saturated.

4.2. Estimate of the average cell delay at the IMA multiplexer

Once a suitable \( \frac{M}{D}/C/(N + C - N_{\text{red}}(C)) \) model has been selected to approximate the IMUX CLR, we want to check whether it also provides a good estimate of the mean waiting time suffered by a cell in the system. Fig. 16 compares the mean waiting time as a function of the offered load at the simulated IMUX and that derived from its equivalent queuing model. In all cases tested, the two average delays exhibit a similar behavior and only differ by a constant value.

In an \( \frac{M}{D}/C/(N + C - N_{\text{red}}(C)) \) model, the minimum cell waiting time (under input load near to zero) is always fixed and equal to 0.5 slots. In an IMA multiplexer, the average cell delay depends on the number of output ports (\( C \)). Accordingly, as a rough approximation, we can add to the analytical results the difference between minimum average delays acquired from the simulated IMUX and the \( \frac{M}{D}/C/(N + C - N_{\text{red}}(C)) \) system.

The minimum average cell delay of an IMUX has two components, one due to the round-robin cell distribution at the IDCR rate and the other caused by the delay that ICP and SICP cells introduce [17]. The first component means that an incoming ATM layer cell is not transmitted before the clocking time at the IDCR rate, although it may be possible that some links be filled with OAM cells at those instants. This delay component can be formulated by (4).

\[
W_{\text{min,IDCR}} = \int_0^1 (1 - x) \, dx + \text{IDCR} \cdot \int_{1/\text{IDCR}}^1 (1 - x) \, dx. \tag{4}
\]

The delay introduced by ICP and SICP cells is due to the fact that the system must always guarantee the delivery of \( C \) outgoing cells (ATM layer, Filler, ICP or SICP), one for each output port at the TRLCR rate. Thus, when a control cell is inserted some ATM layer cell has to wait for its transmission.

The ATM Forum specifies that in an IMA frame ICP cells are located at the offset \( s \), \( s \) being the link number [3,4]. Calculating the average cell delay these cells add into the links [17] yields the expression (8), where \( S(n) \) (6) gives the sending decision times of ATM layer cells into the slot \( n \), and ICP\((n) \) (7) computes the instants for the insertion of ICP cells

\[
 \text{offset}(s) = \frac{2(s + 1) - 2^{\left\lfloor \log_2(s+1) \right\rfloor} - 1}{2^{\left\lfloor \log_2(s+1) \right\rfloor}} M, \quad 0 \leq s \leq C - 1, \tag{5}
\]

\[
S(n) = \sum_{i=1}^{\infty} \delta \left[ n - \left\lfloor \frac{2049}{17 \cdot C} \cdot i \right\rfloor + 1 \right], \tag{6}
\]

\[
\text{ICP}(n) = \sum_{s=0}^{C-1} \left\{ \sum_{k=0}^{\infty} \delta \left[ n - \text{offset}(s) - 2049 \cdot k \right] + \sum_{k=0}^{\infty} \delta \left[ n - \text{offset}(s) - \left\lfloor \frac{127 \cdot C - i}{\text{IDCR}} \right\rfloor \right] \right\} \tag{7},
\]

\[
W_{\text{ICP}}(C) = \frac{1}{C} \frac{1}{2049} \sum_{n=0}^{2049} \left[ \sum_{m=0}^{n} (\text{ICP}(m) - S(m)) \right]. \tag{8}
\]

Consequently, the minimum average cell delay at the IMUX can be described by
\[ W_{\text{min.IMA}} = W_{\text{min.IDCR}} + W_{\text{ICP}}. \] (9)

Once this delay is computed, we approximate the results by the summation of average delays in the \( M/D/C/(N + C - N_{\text{red}}(C)) \) systems plus the difference between minimum average delays \( (\bar{W}_2(C)) \), and these values are further adjusted by simulation \( (\bar{W}_3(\rho, C)) \) is the polynomial of minimum degree that approximates the simulation results achieved.

The resulting expression to estimate the average cell delay at the IMUX is denoted by
\[ \bar{W}_{\text{IMA}}(\rho, C) \approx \bar{W}_{M/D/C/(N - N_{\text{red}}(C))} + \bar{W}_2(C) + \bar{W}_3(\rho, C), \] (10)

where \( \bar{W}_2(C) \) and \( \bar{W}_3(\rho, C) \) are denoted by (11) and (12), respectively,
\[ \bar{W}_2(C) = \bar{W}_{\text{min.IMA}} - \bar{W}_{M/D/C/(N - N_{\text{red}}(C))} = \bar{W}_{\text{min.IMA}} - 0.5, \] (11)
\[ \bar{W}_3(\rho, C) = 0.14626460739\rho - 0.2926126477 \cdot 10^{-2}C + 0.0160573948. \] (12)

Figs. 17 and 18 plot the comparison of simulated and approximated values for an offered load of 60% and 80%, respectively. Confidence intervals are not shown since their values are very small (relative error lower than 2% in all cases).

Given a set of values defining the required QoS, the proposed method allows the dimensioning of the main parameters that characterize an IMUX. For this purpose, the resulting analytical expressions can be used (and their results may be tabulated) instead of developing costly simulations. For instance, employing the figures shown above, let us assume that the maximum mean cell delay and the CLR required are fixed to two time slots and \( 10^{-4} \), respectively, for an offered load per link of 0.8 Erlang. The number of output links needed is 4 lines and the buffer capacity at the IMUX is 24 cells deep. Of course, this is true if the Poisson input traffic hypothesis holds. Another planning situation can be, for a fixed number of links (e.g., 2 links), to obtain the maximum offered load per link to keep the average cell delay lower than 3 slots, a CLR lower than \( 10^{-4} \) and 20 cells of storage. In this case, the maximum applicable load per link is 0.7 Erlang and the total load offered to the IMUX 1.4 Erlang. Similarly, the IDCR and TRLCR rates can be dimensioned taking into consideration the offered load per link.

5. Performance evaluation under bursty traffic

One of the main advantages of ATM is its ability to perform statistical multiplexing combining several traffic sources on a single connection. However, to achieve some statistical multiplexing gain, a sufficient number of uncorrelated traffic sources have to be multiplexed. This technique is especially relevant if traffic sources are bursty.

Integrated traffic that circulates on ATM networks is generated by sources of differing nature.
A significant part of it shows high variability and appears in batches [12]. Some traffic patterns have been proposed to characterize bursty traffic generated by video and data traffic sources. In addition, network traffic measures have been published that in some cases indicate a self-similar behavior. However, the analytical models to define this type of traffic sources are too complex and they are not well accepted yet. Indeed, it is still an open research area. Here, we are interested in simple models capturing the bursty property of some sources.

Congestion control is one of the main problems for supporting bursty traffic. A relatively long traffic burst may saturate buffers at the network nodes, degrading the QoS demanded by network connections. To minimize these adverse effects on the network, preventive (i.e., connection admission control (CAC) and usage parameter control (UPC)) and reactive measures are exerted on the traffic. These mechanisms are not used in our simulations.

In this section, two bursty traffic models are employed only as a rough approximation to gain some insight into the behavior of IMA systems to support this type of traffic, but as was stated above, it is not the main issue of this work. The first model degrades IMA performance depending on the active and idle period length, but under certain conditions it is still possible to apply the dimensioning rules developed for Poisson traffic. The second model characterizes traffic on residential networks [11]. It is interesting because for these networks a cost-effective solution to access ATM services can be applied using IMA. Under this traffic even for low loads, the necessary buffering size to maintain a given QoS is high.

5.1. On–off traffic

IMA specifies the multiplexing and de-multiplexing of ATM cells in round-robin fashion among a group of links creating a higher bandwidth virtual link that operates at the IDCR rate. The IDCR is a constant cell rate that depends on the number of output links. In Section 4, it was explained that the insertion of IMA protocol cells and the cyclic distribution introduce delay and CDV, causing the effective occupation of the IMUX buffers to be higher than expected.

Traffic is offered to an input link operating at a given transfer rate (in all simulations a transfer rate of 34 Mbps is taken, corresponding to an E3 link). The offered traffic arrives in batches, and a two-state Markov chain, which alternates between active and idle periods, models it. The active and idle period length follow a random geometric distribution of mean $T_{on}$ and $T_{off}$, respectively. The minimum active period length is of one cell-length. The minimum idle period length can be zero. No cell generation occurs during the idle period and cells are generated during active periods according to Bernoulli trials of probability $a$ [6], as represented in Fig. 19.

The load applied to the input link is given by

$$\rho_{\text{link}} = \frac{T_{on}}{T_{on} + T_{off}} a, \quad 0 \leq a \leq 1. \quad (13)$$

Therefore, the offered load applied to the IMUX is

$$\rho_{\text{IMA}} = \frac{\lambda}{\text{IDCR}} = \frac{\rho_{\text{link}} \cdot \text{E3 cell rate}}{\text{IDCR}}. \quad (14)$$

The on–off traffic increases the buffer occupation during the $T_{on}$ period if its peak cell rate (PCR) is greater than the IMA output rate (IDCR). Here, we analyze the IMUX performance under on–off traffic. It is assumed that the IMUX is fed by an E3 link running at 34 Mbps. This guarantees that ATM cells can arrive at a higher rate than the output one (since no more than 8 output links are considered). A lower rate does not need memory to store cells. In the simulations, the E3 input link loads the IMUX with a factor varying from 50% to 90%.

In this study, the mean length of the active period was 32 cells (approximately the length of an Ethernet frame) and the idle period was adjusted to achieve the desired load.

![Fig. 19. On–off bursty traffic model.](image-url)
Figs. 20 and 21 plot the CLR obtained for \( C \) up to 8 IMUX output ports. The 95% confidence intervals are also shown. It can be observed that the CLR decreases as the buffer size increases. This fact becomes more important at low loads. In addition, contrary to the Poisson traffic case, the CLR decreases as the number of links enlarges. This is because the input traffic load grows, but this growth is accomplished only by decreasing the \( T_{\text{off}} \) period. \( T_{\text{on}} \) is the same as the cell generation rate during the active period. However, acting this way, the applied load per link is not kept constant. Therefore, if the number of links is higher the capacity to serve cells is also higher and the CLR for the same amount of buffering decreases.

Figs. 22 and 23 depict the average cell delay obtained by simulation from the time a cell enters the buffer to its exit from the system. The results are for \( C \) ranging from 2 to 8 output links, applied loads of 60% and 80% and variable buffer sizes. The confidence intervals are not shown since they are too small.

The average cell delay decreases as \( C \) increases. Its value tends to a constant, as the buffer size takes higher values. This is because the average number of cells in the system is lower than the buffer size. As the offered load increases, the average cell delay likewise increases, since the buffer suffers more occupation.

Comparing these results to the ones obtained under Poisson cell arrivals (Section 4), it can be noticed that for on-off traffic over an E3 input link with \( T_{\text{on}} = 32 \), the CLR and average cell delay values are very different. Nevertheless, we observed in [17] that for lower values of \( T_{\text{on}} \) (<10) and \( T_{\text{off}} \) the dimensioning method using Poisson traffic still holds (Fig. 24 shows an example of CLR for an applied load of 80%, with \( T_{\text{on}} = 6 \) and \( T_{\text{off}} = 4 \)). Note that in this case the CLR increases.
with the number of links and the values are near those for Poisson traffic. This is due to the similarity of these traffics when the idle periods are shorter (e.g., several on–off traffic source aggregation).

5.2. WWW traffic model in residential networks

A network is installed in homes to connect several devices to shared resources and provide residential equipment with access to telecommunication services offered through an access network. It is assumed that the equipment attached to a “normal” residential network is a TV set with its corresponding set-top box, a PC station, a printer and a digital telephone set. The traffic that circulates over these networks can be internal and external. Internal traffic has its origin and destination on the residential network. External traffic is that addressed from the access network to the home or in the opposite direction (usually the latter is negligible). The access network can be based on hybrid-coaxial technology (HFC), asymmetric digital subscriber loop (ADSL and xDSL variations) or by means of IMA for direct access to B-ISDN services. Data traffic patterns for a residential network are quite different to those in corporate environments [11]. At home, Poisson or self-similar traffic arrival processes are unlikely to be found because there are not so many hosts; therefore, the usual infinite population assumption does not hold. The composition of the network is also different, network file servers and diskless stations being uncommon. In addition, the network load is expected to be smaller since the foreseeable services and applications are not so powerful as in a corporate scenario. Here, the traffic is basically external, for accessing services outside, while in a corporate environment the highest percentage tends to be internal traffic. All these aspects imply different traffic profiles for residential data traffic.

Given this situation, in [11] an Ethernet residential network is taken as the most feasible option due to its widespread use and low cost. Residential traffic is characterized by monitoring real traffic circulating on the network and further approximated by a statistical model. In particular, the external WWW traffic is modeled in [11] by a Pareto distribution characterizing the message sizes of the document retrieval service and a Weibull distribution for the inter-retrieval times.

1) Distribution of the document sizes: This is based on the distribution of the available files on a specific service, for instance on a WWW service. The studies found in [10] show that the message transfer size can be modeled by a Pareto distribution, whose probability density function is given

\[ P(x) = \beta R^\beta x^{-\beta-1}, \]  

where \( R \) is the minimum value of the random variable \( x \) (document size) and \( \beta \) determines the shape of the distribution. The distribution function used in the simulations is denoted by (16). According to [10], \( \beta \) and \( R \) take the following values, \( \beta = 1.03 \) and \( R = 1 \) KB.

\[ F(x) = \Pr(I \leq x) = 1 - \left( \frac{R}{x} \right)^\beta. \]  

(16)

2) Distribution of the document inter-retrieval times: Assuming the research developed in [10,11,16], the inter-retrieval time \( T \) is characterized by a Weibull distribution whose probability density function is

\[ P(T) = k \left( \frac{T}{\theta} \right)^{k-1} e^{-(T/\theta)^k}. \]  

Its distribution function responds to the expression

\[ F(T) = \Pr(t \leq T) = 1 - e^{-(T/\theta)^k}. \]  

(18)
The parameters used are $k = 0.5$ and $\theta = e^{1.5}$ [11], but only values of less than 60 s are taken into consideration.

This traffic is generated over an E3 link, and the resulting traffic is also bursty. A representation of this traffic type is shown in Fig. 25. In consequence, the active period is given by the selected Pareto distribution and the sum of the active and idle periods depends on the time between messages obtained from the above-mentioned Weibull distribution.

The source generates first the size of the document (i.e., Pareto distribution) and segments it into ATM cells with 48 bytes of data (i.e., using Multiprotocol Encapsulation over AAL5 [13]). The interarrival time is generated as a Weibull random variable, and transformed into slots. If the active period exceeds the interarrival period, then they are computed again. In this paper, we take the values studied in [11]. In particular, the message size follows a Pareto distribution with $\beta = 1.03$ and minimum size $R = 1$ kilobyte. The mean size value is

$$m_x = \int_R^\infty x \cdot \left(\beta R^\beta x^{-\beta - 1}\right) \, dx = R \cdot \frac{\beta}{\beta - 1}$$

$$= 34,333 \text{ bytes.} \tag{19}$$

Assuming that data coming from Ethernet frames are segmented into ATM cells completely filling their information field (48 octets), it produces, on average, a burst of approximately 716 cells. This traffic from a 10 Mbps Ethernet is injected into the IMUX at E3 bit rate, thus, the average active period length is around 27.5 ms. The mean time between two consecutive message arrivals is computed by a Weibull distribution of parameters $k = 0.5$ and $\theta = e^{1.5}$. This value for $\beta > 1$ can be obtained from [15] and is shown in (20)

$$m_x = \theta \cdot \gamma^{1-k} \cdot \Gamma \left(1 + \frac{1}{k}\right) = 0 \cdot \Gamma(3)$$

$$= 8.96 \text{ s.} \tag{20}$$

Using the above, the load offered to the input link at E3 bit rate can be expressed by (21). This implies a load offered to the IMUX device given by (22)

$$\rho_{E3} = \frac{\text{Cells arriving in } T_{on}/(T_{on} + T_{off})}{E3 \text{ cell rate}}$$

$$= \frac{716 \text{ cells/8.96 s}}{8.85 \times 10^4 \text{ cells/s}} = 0.09025\%,$$ \quad (21)

$$\rho_{IMA} = \frac{E3 \text{ cell rate}}{1.55 \text{ IDCR}} \cdot \frac{\rho_{E3}}{\text{IMA output links}} \%.$$ \quad (22)

Note that the load applied to the IMA multiplexer is very low and it decreases as the number of links increases. $T_{on}$ depends on the input link data rate; if this rate rises $T_{on}$ falls and the number of ATM cell arrivals during $T_{on}$ grows in the same proportion, also increasing the buffer occupation.

Since the load applied to the IMUX under these conditions is low, it means that the CLR basically depends on the received message length (716 cells on average). Another important factor is the variance of the message length, which is infinite for a Pareto distribution. A priori, this suggests that the cell losses may be high and difficult to reduce.

Figs. 26 and 27 plot the CLR and average cell delay for this input traffic, 2, 3 and 4 output links.
and a buffer capacity varying from 1000 to 10,000 cells.

As expected, the CLR is very high and decreases slowly even for large buffer sizes. This effect does not occur for Poisson input traffic (even for high loads (90%)), since cell arrivals are distributed more evenly in time, and therefore, the IMUX is able to serve a higher number of cells. Here, the arrival of a cell burst is at the input link rate, notably higher than the output bit rate. Hence, the accumulation and storage of cells is unavoidable. The memory required becomes greater for higher input link bit rates and higher average length of active periods. Of course, as the number of output links grows the service rate (IDCR) also grows and the CLR is reduced.

The average cell delay depends on the number of cells being stored in the system. It grows in accordance with the buffer size. There is a noticeable trend to stabilize to a constant value because the applied load does not exceed 100%. Therefore, taking a sufficiently large buffer size, a maximum average delay can be obtained. Again, for a greater number of output lines the average cell delay becomes smaller, since the system transmits cells at a higher rate, thus decreasing the buffer occupancy. In comparison to Poisson input traffic, it can be observed in Fig. 27 that the average cell delay is much greater, as is to be expected with a higher number of cells to store.

Consequently, the method to dimension IMUX resources developed under Poisson traffic does not apply directly for this residential traffic model. However, it is expected that this traffic will be multiplexed with various similar sources coming from other homes before it tackles the IMUX input. In this case, the behavior tends to improve.

6. Concluding remarks and future work

In this paper, inverse multiplexing for ATM and its primary network applications are described. IMA provides an economical alternative to the bandwidth gap between T1/E1 and T3/E3. Using IMA, two or more T1/E1 can be combined to create a single logical connection with an effective bandwidth of multiple T1/E1 lines. ATM cells are multiplexed and de-multiplexed in round-robin fashion among an IMA group of output links. IMA represents a physical layer technology; therefore, it can be used to transport any service once it has been adapted to ATM cell format.

To fulfill its function in both directions of communication, IMA builds IMA frames and inserts control cells (ICP, SICP and Filler cells). These allow the introduction of time markers to recover the original ATM layer cell stream, cell decoupling rate function and synchronism operations.

To study the behavior and evaluate the performance of IMA systems a flexible and object-oriented simulation tool has been developed. IMA multiplexers have been characterized and analyzed under Poisson input traffic. First, the CLR as a function of the offered load and number of output links is investigated. An equivalent \( M/D/C/(N + C) \) queue model is used to propose a method to dimension the memory required at the IMUX. Reducing the queue size of this analytical model, an accurate approximation to the simulation results is obtained. The queuing system is further manipulated to adjust the average cell delay. The fit achieved is good enough, although the method is dependent on the simulation results. We are currently working towards mathematical approximations and exact solutions of \( M/D/1/N \) queue systems and obtaining very promising results, regarding both CLR and average cell delay. In these cases, the need to conduct costly simulations is completely obviated.
Preliminary results for two types of bursty traffic patterns have also been presented. These traffic models are characterized by the generation of cells in active periods and inactivity during idle periods. In general, more buffering is needed to cope with this traffic. In some cases, the amount of memory is prohibitive and performance does not improve on increasing it.

Under on–off traffic and for short and medium bursts the proposed methodology to dimension IMUX resources is still valid. However, when the injected traffic is a characterization of WWW services over residential networks the amount of memory required at the IMUX for a given QoS is excessive. This is due to long active periods compared to the time slot in the output lines, even for low applied loads (<1%). Nevertheless, IMUX performance depends on the input traffic pattern. This also holds for any network node. Using Poisson traffic is almost the only way to obtain analytical models and closed mathematical expressions. Although Poisson traffic is not a realistic pattern for access network nodes and for the current traffic measured in ATM networks, it is still a useful approach to validate the characterization and simulation models of these ATM network nodes. Only a few years ago, no one forecasted the current traffic patterns on the Internet, mainly WWW traffic. Therefore, the actual traffic behavior is subject to near future changes in user behavior, resulting in self-similar patterns or others. However, operators, network planners and traffic engineers will continue developing device node libraries to incorporate more or less complex network simulators. These simulators will be fed with realistic traffic patterns according to users’ changing needs. However, it is highly probable that engineers will still use easy and useful patterns, such as the Poisson one, to validate and verify their newly developed simulators. This is why we still believe in the usefulness of a “permanent” and understandable traffic pattern to study the IMUX and to analyze it mathematically [1,18]. In this paper, we show the changing behavior of our ATM IMUX node for other input traffic for the sake of being complete.

It can be concluded that the dimensioning procedure proposed is reliable enough for short and medium length active periods. At present, we are examining the actual degree of correctness and the extrapolation of results under different bursty traffic patterns, together with possible solutions when the method does not hold. The new patterns to investigate consider single and multiplexed traffic sources. Simple but realistic traffic patterns that are understandable by network planners are especially relevant to our research.

Finally, another part of our current work is the incorporation of different traffic classes into the simulation environment (CBR, VBR-rt, VBR-nrt, ABR and UBR). This will involve some changes in the buffering schemes used and the addition of scheduling mechanisms to handle ATM cells. In this new and more realistic framework, we will extend our analysis to approximate the performance offered by IMA systems.

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References


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